CLAIMS

What is claimed is:

1. A computer system, comprising:

a microprocessor coupled to a primary bridge device;

a main memory array coupled to a memory controller by way of a memory bus, said memory controller integral with said primary bridge device;

a secondary bridge device coupled to said primary bridge device by way of a primary expansion bus;

an input/output controller coupled to said secondary bridge device by way of a secondary expansion bus;

a read only memory (ROM) coupled to said secondary bridge device by way of the secondary expansion bus, said ROM stores programs executable by the microprocessor;

a keyboard coupled to said input/output controller;

a host clock generator having a host clock signal coupled to a phase locked loop (PLL) device and said memory controller;

said PLL device having a plurality of PLL output signals having the same frequency as the host clock output signal, but differing in phase relationship;

one of said PLL outputs signals coupled to said main memory array, and one of said PLL output signals coupled to said memory controller;

a clock delay circuit coupled between said PLL output signal and said memory controller, said clock delay circuit time delays said PLL output signal, said clock delay circuit comprising:

a first signal path having a first length, said first signal path selectable by a first electrically controlled switch coupled to the first signal path; and

a second signal path having a length longer than said first length, said second signal path selectable by a second electrically controlled switch coupled to the second signal path;

wherein said clock delay circuit routes said PLL output signal along one of said first signal path for a short time delay, and said second signal path for a long time delay.

2. The computer system as defined in claim 1 wherein said electrically controlled switches further comprise field effect transistors (FETs), thereby creating a first and second FET coupled to the first and second signal paths respectively.

3. The computer system as defined in claim 2 further comprising:

a gate of said first FET coupled to an output signal of a control device;

a gate of said second FET coupled to an output signal of the control device;

the output signals of said control device are selectively asserted and de-asserted by command of software instructions stored on said ROM device and executed by said microprocessor; and

wherein the assertion and de-assertion of the output signals acts to select one of the first and second signal paths.

4. The computer system as defined in claim 3 wherein the control device further comprising said secondary bridge device.

5. The computer system as defined in claim 3 wherein the control device further comprising said input/output controller.

6. The computer system as defined in claim 3 wherein said software instructions stored on said ROM determines a number of dual inline memory modules (DIMMs) present in the main memory array of said computer system, and configures the time delay implemented by the clock delay circuit based on the number of DIMMs by asserting and de-asserting outputs of said control device.

7. The computer system as defined in claim 6 wherein said software instructions on said ROM device further comprises a look-up table that indicates the selection of one of the first and second signal paths as a function of the number of DIMMs present in the main memory array of the computer system.

8. The computer system as defined in claim 6 wherein said software instructions on said ROM tests each path of the first and second signal of said clock delay circuit to determine a shortest possible path length to implement as a function of which path length is the shortest useable length without invoking bit errors in data transfers.

9. The computer system as defined in claim 6 wherein said control device is the secondary bridge device.

10. The computer system as defined in claim 3 wherein said output signals of said control device further comprise digital output signals.

11. The computer system as defined in claim 1 further comprising:

a phase lag circuit coupled within a feedback path of the PLL device adjusts the phase of the PLL output signals in relation to the host clock signal by selectively implementing different lengths of the feedback path by the selective assertion of one of a plurality of electrically controlled switches, said switches coupled one each to a plurality of feedback signal paths of varying lengths.

12. The computer system a defined in claim 11 wherein said plurality of feedback signal paths of varying lengths further comprise:

a first feedback signal path having a length coupled to and selectable by a first feedback FET; and

a second feedback signal path having a length longer that said first feedback signal path, said second feedback signal path coupled to and selectable by a second feedback FET.

13. The computer system as defined in claim 12 further comprising:

a gate of said first feedback FET coupled to an output signal of a control device;

a gate of said second feedback FET coupled to an output signal of the control device; and

wherein said ROM device stores software instructions, executed by said microprocessor, which selectively assert one of the output signals of the control device to implement the feedback path with a length that includes one of said first and second signal paths.

14. The computer system as defined in claim 13 wherein said selective assertion of output signals by the software instructions is based on a required phase lag between the host clock signal and the PLL output signals as a function of parasitic capacitance present on the memory bus.

15. The computer system as defined in claim 13 wherein said control device further comprises the secondary bridge device.

16. The computer system as defined in claim 13 wherein said control device further comprises the input/output controller.

17. A method of adaptively compensating for parasitic capacitance on a bus transferring data from a sending device to a receiving device, comprising:

coupling a plurality of signal paths, at least two of the plurality having different path lengths, between a source of a read clock and the receiving device, which receiving device uses the read clock as a trigger to read data from the bus;

selecting one of the signal paths, based at least in part on the parasitic capacitance, by forcing an electrically controlled switch into a conduction mode, for the path desired, and by forcing remaining electrically controlled switches, associated with other paths, into a non-conductive mode; thereby

adjusting a phase relationship between the read clock and a write clock, used by the sending device as a trigger to drive data to the bus.

18. The method as defined in claim 17 wherein forcing the electrically controlled switches into conductive and nonconductive modes further comprises:

asserting a first output signal of a control device coupled to a gate connection of a first FET, and substantially simultaneously deasserting a second output signals of the control device coupled to a gate connection of a second FET; thereby

passing the read clock through the first FET and one of said plurality of signal paths; and

preventing the passage of the read clock through the second FET, thereby disallowing propagation of said read clock through remaining signal paths of the plurality of signal paths.

19. The method as defined in claim 18 wherein selecting one of the signal paths further comprises:

determining a number of dual inline memory modules (DIMMs) present in said sending device; and

referring to a look-up table which directs the use of one of said signal path based on the number of DIMMs present.

20. The method as defined in claim 18 wherein selecting one of the signal paths further comprises determining a shortest signal path length of the read clock at which data transfers between the sending device and the receiving device occur without error.

21. The method as defined in claim 20 wherein determining the shortest signal path length further comprises:

testing each signal path from a longest path length to the shortest path length by transferring test data from the sending device to the receiving device and checking for bit errors,

said testing continued until the signal path length used for the read clock causes bit errors in the transfer of the test data; and

selecting a path length for the read clock at which no bit errors occurred in the transfer of test data.

22. A system to control phase lag of clock signals within a computer system, comprising:

a host clock device having a host clock (HCLK) output signal;

said HCLK output signal coupled to an input signal of a phase locked loop (PLL) device and an input signal of a memory controller;

a main memory array coupled to said memory controller by way of a memory bus, said memory array comprising at least one dual inline memory module (DIMM), said DIMM coupled to and adding a parasitic capacitance to the memory bus;

a PLL output clock signal coupled to said memory controller, said memory controller adapted to read data on said memory bus responsive to said PLL output clock signal;

a read clock (RDCLK) delay circuit coupled between the PLL output clock signal and the memory controller;

at least one control signal coupled to said RDCLK delay circuit; and

wherein the RDCLK delay circuit selectively implements varying length paths for the RDCLK signal responsive to the control signal.

23. The system to control phase lag of clock signals within a computer system as defined in claim 22 wherein said RDCLK delay circuit further comprises:

a first signal path having a first length, said first signal path selectable by a first electrically controlled switch coupled to the first signal path;

a second signal path having a length longer than said first length, said second signal path selectable by a second electrically controlled switch coupled to the second signal path;

each of said electrically controlled switches having a control input connection coupled to the control signal; and

wherein said clock delay circuit routes the PLL output signal along one of said first signal path for a short phase delay, and said second signal path for a long phase delay.

24. The system to control phase lag of clock signals in a computer system as defined in claim 23 wherein the electrically controlled switches of said RDCLK delay circuit further comprise:

field effect transistors (FETs), each having a gate connection; and

the control signal coupled to the gate of each FET.

25. The system to control phase lag of clock signals in a computer system as defined in claim 24 further comprising:

an output signal of a bridge device coupled to the at least one control signal;

a software program executed by a microprocessor selectively asserting the output signal of the bridge device based, at least in part, on a number of DIMMs present in said computer system.

26. The system to control phase lag of clock signals in a computer system as defined in claim 23 further comprising:

a first FET having its drain coupled to a first end of the first signal path, and a second FET having its source coupled to a second end of the first signal path;

a third FET having its drain coupled to a first end of the second signal path, and a fourth FET having its source coupled to a second end of the second signal path;

gate connections of the first and second FETs coupled to each other, and further coupled to the at least one control signal;

gate connections of the third and fourth FETs coupled to each other, and further coupled to the at least one control signal; and

the RDCLK delay circuit implements the first signal path when said first and second FETs are in a conductive mode responsive to the at least one control signal, and said RDCLK delay circuit further implements the second signal path when said third and fourth FETs are in a conductive mode responsive to their gates signal.

27. The system to control phase lag of clock signals in a computer system as defined in claim 23 further comprising:

the gate connections of the first and second FETs coupled to a first control signal;

the gate connections of the third and fourth FETs coupled a second control signal;

each of said first and second control signals coupled to output signals of a control device; and

wherein said output signals of the control device are selectively asserted and de-asserted by a software program, executed by a microprocessor.

28. The system to control phase lag of clock signals in a computer system as defined in claim 27 further comprising:

the control device is a secondary bridge device; and

the software program is stored on a read only memory coupled to said secondary bridge device.

29. The system to control phase lag of clock signals in a computer system as defined in claim 22 further comprising:

said PLL device having a feedback path, the length of said feedback path controls the phase relationship between the input signal of the PLL device and PLL output signals; and

a feedback delay circuit coupled within the feedback path of the PLL device, said feedback delay circuit adapted to selectively change the length of said feedback path, said feedback delay circuit comprising:

a first feedback path having a length, said first feedback path selectable by a first electrically controlled switch coupled to the first feedback path; and

a second feedback path having a length longer than the length of the first feedback path, said second feedback path selectable by a second electrically controlled switch coupled to the second feedback path.

30. A method of adaptively controlling phase shift of clock signals in a computer system, comprising:

coupling a host clock signal to a phase locked loop (PLL) device, and a memory controller;

coupling the memory controller to a main memory array;

coupling a first PLL output signal to a variable length clock path circuit;

coupling a variable length clock path circuit output signal to the memory controller;

adjusting a length of a clock path through said variable length clock path circuit so as to selectively time delay the variable length clock path output signal relative to the first PLL output signal, wherein said adjusting further comprises:

activating a first electrically controlled switch to select a first clock path having a desired length; and

refraining from activating a second electrically controlled switch and thereby not selecting a second clock path.

31. The method as defined in claim 30 further comprising:

implementing a variable length feedback path circuit in a feedback path of the PLL device;

determining the number of dual inline memory modules (DIMMs) present in a main memory array;

adjusting the length of the feedback path of the PLL device as a function of the number of DIMMs to adjust the phase relationship between the host clock signal and PLL output signals, said adjusting accomplished by selecting one of a plurality of possible path lengths in the variable length feedback path circuit by actuating an electrically controlled switch.

32. A system to control phase lag of clock signals within a computer system, comprising:

a host clock device having a host clock (HCLK) output signal;

said HCLK output signal coupled to an input signal of a phase locked loop (PLL) device and an input signal of a memory controller;

a main memory array coupled to said memory controller by way of a memory bus, said memory array comprising at least one dual inline memory module (DIMM), said DIMM coupled to and adding a parasitic capacitance to the memory bus;

a PLL output clock signal coupled to said memory controller, said memory controller adapted to read data on said memory bus responsive to said PLL output clock signal;

said PLL device having a feedback path, the length of said feedback path controls the phase relationship between the input signal of the PLL device and PLL output signals;

a feedback delay circuit coupled within the feedback path of the PLL device;

at least one control signal coupled to said feedback delay circuit;

said feedback delay circuit selectively changes the length of said feedback path responsive to the control signal.

33. The system to control phase lag of clock signals within a computer system as defined in claim 32 wherein said feedback delay circuit further comprises:

a first signal path having a first length, said first signal path selectable by a first electrically controlled switch coupled to the first signal path;

a second signal path having a length longer than said first length, said second signal path selectable by a second electrically controlled switch coupled to the second signal path;

each of said electrically controlled switches having a control input connection coupled to the control signal; and

wherein said feedback delay circuit routes the PLL feedback path along one of said first signal path for a short phase delay, and said second signal path for a long phase delay.

34. The system to control phase lag of clock signals in a computer system as defined in claim 33 wherein the electrically controlled switches of said feedback delay circuit further comprise:

field effect transistors (FETs), each having a gate connection; and

the control signal coupled to the gate of each FET.

35. The system to control phase lag of clock signals in a computer system as defined in claim 34 further comprising:

an output signal of a bridge device coupled to the at least one control signal;

a software program executed by a microprocessor selectively asserting the output signal of the bridge device based, at least in part, on a number of DIMMs present in said computer system.

36. The system to control phase lag of clock signals in a computer system as defined in claim 33 further comprising:

a first FET having its drain coupled to a first end of the first signal path, and a second FET having its source coupled to a second end of the first signal path;

a third FET having its drain coupled to a first end of the second signal path, and a fourth FET having its source coupled to a second end of the second signal path;

gate connections of the first and second FETs coupled to each other, and further coupled to the at least one control signal;

gate connections of the third and fourth FETs coupled to each other, and further coupled to the at least one control signal; and

the feedback delay circuit implements the first signal path when said first and second FETs are in a conductive mode responsive to the at least one control signal, and said feedback delay circuit further implements the second signal path when said third and fourth FETs are in a conductive mode responsive to their gates signal.

37. The system to control phase lag of clock signals in a computer system as defined in claim 36 further comprising:

the gate connections of the first and second FETs coupled to a first control signal;

the gate connections of the third and fourth FETs coupled a second control signal;

each of said first and second control signals coupled to output signals of a control device; and

wherein said output signals of the control device are selectively asserted and de-asserted by a software program, executed by a microprocessor.

38. The system to control phase lag of clock signals in a computer system as defined in claim 37 further comprising:

the control device is a secondary bridge device; and

the software program is stored on a read only memory coupled to said secondary bridge device.

39. The system to control phase lag of clock signals in a computer system as defined in claim 32 further comprising:

a read clock (RDCLK) delay circuit coupled between the PLL output clock signal and the memory controller;

at least one control signal coupled to said RDCLK delay circuit; and

wherein the RDCLK delay circuit selectively implements varying length paths for the RDCLK signal responsive to the control signal, said RDCLK delay circuit comprising:

a first clock path having a length, said first clock path selectable by a first electrically controlled switch coupled to the first clock path; and

a second clock path having a length longer than the length of the first clock path, said second clock path selectable by a second electrically controlled switch coupled to the second clock path.